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EXAMINER	
DUONG, FRANK	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,971	KLAUSMEIER ET AL.	
	Examiner	Art Unit	
	Frank Duong	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,17,19-26,31 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,17,19,20,23,25,26,31 and 34* is/are rejected.

7)☒ Claim(s) *21, 22, 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to communications dated 06/16/05. Claims 16-17, 19-26, 31 and 34 are pending in the application.

Terminal Disclaimer

2. The terminal disclaimer filed on 06/16/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of patent No. 6,343,075 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Objections

3. Claim 26 is objected to because of the following informalities: Line 2, "may be" should change to --is--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Zola (USP 4,400,627) (hereinafter "Zola").

Regarding **claim 25**, in accordance with Zola reference entirety, Zola shows a rearrangeable, non-blocking, three-stage switch configured as a Clos network (Fig. 4), said switch comprising:

a plurality of physical center stage switch circuits, a number of said plurality of physical center stage switch circuits equaling N, where N is an integer other than a power of 2 (*see Fig. 4 for connection and description at col. 5, lines 43-45. Three Center Stage Switches 201-203 are provided. Thus, three is not a power of 2*);

a plurality of logical center stage switch circuits equaling N*f, where f is a number of logical center stage switch circuits per physical center stage switch circuit, wherein the plurality of physical center stage switch circuits are configured into the plurality of logical center stage switch circuits (*col. 5, line 60 to col. 6, line 22, Zola discloses the connection process for using two or more center stage switches*); and

a subset of the plurality of logical center stage switch circuits equaling n, where n is less than N*f and n is a power of 2 (*Fig. 4 shows center stage switches 201-203 and at col. 5, lines 45-52, Zola shows with certain input connections only two center stage switches 201-202 are used and 2 is a power of 2*).

As per **claim 26**, the limitation of "wherein the subset of the plurality of logical center stage switch circuits initially carries no data signals and may be used as spares" calls for a negative (i.e., "carries no data") and made optional (i.e., "may be") limitation. Thus, it is anticipated by Zola reference.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16-17, 19-20, 23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zola in view of Andresen (The Looping Algorithm Extended to Base 2^t Rearrangeable Switching Networks, IEEE, pages 1057-1063, 1977) (hereinafter "Andresen").

Regarding **claim 16**, in accordance with Zola reference entirety, Zola discloses a rearrangeable, non-blocking switch (Fig. 4), comprising: a first stage (Input Stage Switches 101-164) including a plurality of first switch circuits (101-164), each of said plurality of first switch circuits including a plurality of inputs and a plurality of outputs (*see Fig. 4 for connections and description at col. 5, lines 33-43*); a second stage (Center Stages Switches 201-203) including a plurality of second switch circuits (201-203), each of said plurality of second switch circuits including a plurality of inputs, each of which being respectively coupled to one of said plurality of outputs of each of said plurality of first switch circuits, and a plurality of outputs, a number of said plurality of second switch circuits equaling N, where N is an integer other than a power of 2 (*see Fig. 4 for connection and description at col. 5, lines 43-45. Three Center Stage Switches 201-203 are provides. Thus, three is not a power of 2*); and a third stage (Output Stage Switches 301-364) including a plurality of third switch circuits, each of

said plurality of third switch circuits including a plurality of inputs and a plurality of outputs, each of said plurality of inputs of each of said plurality of third switch circuits being coupled to a respective one of said plurality of outputs of each of said plurality of second switch circuits (*see Fig. 4 for connections and description at col. 5, lines 55-59*), wherein at least some of said plurality of second switch circuits (201-203) are each configured as a plurality of logical switch circuits (*connection process of the switches is discussed at col. 5, line 60 col. 6, line 22*). Zola discloses all of the limitations discussed above, but fails to further disclose "*wherein a Looping Algorithm is used as a control algorithm for the switch*". However, such limitation lacks thereof from Zola reference is well-known as proposed by Waksman, dubbed by Tsao-Wu and extended to the case of $m= 2^t$ in the above technical paper disclosed by Andresen.

In accordance with Andresen reference entirety, Andresen discloses control algorithm for the switch in Clos networks is Looping Algorithm to provide a routing procedure gives control data applicable to base 2^t (see abstract and thereinafter).

Thus, it would have been obvious to those skilled in the art, at the time of the invention was made, having the references of Zola and Andresen readily available, to implement the Looping Algorithm into Zola's switch to arrive the claimed invention with a motivation to provide a routing procedure gives control data applicable to base 2^t (see abstract and thereinafter).

Regarding **claim 17**, in addition to features recited in base claim 16, Zola in view of Andresen further discloses wherein at least one of the plurality of logic switch circuits does not carry data in order to configure the at least some of said plurality of second

switch circuits as n logical switch circuits, where n is a power of 2 ('627, *col. 5, lines 49-50, Zola discusses the output terminals of input stage switches 102-104 are connected to two center stage switches 201-201 (2 is a power of 2), while center stage switch 203 is available*).

Regarding **claim 19**, in addition to features recited in base claim 16, Zola in view of Andersen further discloses wherein each of said plurality of first and third switch circuits are configured to be logically represented as respective grouping of 2x2 switches ('627, *see Fig. 4. It is noted that this limitation is a common in Clos network*).

Regarding **claim 20**, in addition to features recited in base claim 16, Zola in view of Andresen further discloses wherein each of said plurality of outputs of said plurality of first switch circuits, outputs a respective one of a plurality of data signals, said data signals being time-division multiplexed ('627, see *Fig. 4 and col. 5, line 35-37*).

Regarding **claim 23**, in addition to features recited in base claim 16, Zola in view of Andresen further discloses wherein each of said plurality of outputs of said plurality of switch circuits, outputs a respective one of a plurality of data signals, said data signals being multiplexed ('627, see *Fig. 4 and col. 5, line 35-37*).

Regarding **claim 34**, in accordance with Zola reference entirety, Zola shows a rearrangeable, non-blocking, three-stage switch configured as a Clos network (Fig. 4), said switch comprising: a plurality of physical center stage switch circuits, a number of said plurality of physical center stage switch circuits equaling N, where N is an integer other than a power of 2 (*see Fig. 4 for connection and description at col. 5, lines 43-45. Three Center Stage Switches 201-203 are provides. Thus, three is not a power of 2*);

a plurality of logical center stage switch circuits equaling N*f, where f is a number of logical center stage switch circuits per physical center stage switch circuit, wherein the plurality of physical center stage switch circuits are configured into the plurality of logical center stage switch circuits (*col. 5, line 60 to col. 6, line 22, Zola discloses the connection process for using two or more center stage switches*); and a subset of the plurality of logical center stage switch circuits equaling n, where n is less than N*f and n is a power of 2 (*Fig. 4 shows center stage switches 201-203 and at col. 5, lines 45-52, Zola shows with certain input connections only two center stage switches 201-202 are used and 2 is a power of 2*). Zola discloses all of the limitations discussed above, but fails to further disclose "*wherein a Looping Algorithm is used as a control algorithm for the switch*". However, such limitation lacks thereof from Zola reference is well-known as proposed by Waksman, dubbed by Tsao-Wu and extended to the case of $m= 2^t$ in the above technical paper disclosed by Andresen.

In accordance with Andresen reference entirety, Andresen discloses control algorithm for the switch in Clos networks is Looping Algorithm to provide a routing procedure gives control data applicable to base 2^t (see abstract and thereinafter).

Thus, it would have been obvious to those skilled in the art, at the time of the invention was made, having the references of Zola and Andresen readily available, to implement the Looping Algorithm into Zola's switch to arrive the claimed invention with a motivation to provide a routing procedure gives control data applicable to base 2^t (see abstract and thereinafter).

6. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zola in view of Gao et al (UPS 5,945,922) (hereinafter "Gao").

Regarding **claim 31**, Zola discloses the claimed features of base claim 25 (see rationales discussed above), but fails to further disclose "*wherein each of the plurality of physical center stage switch circuits is comprised of a second three-stage switch*". However, such limitation lacks thereof from Zola is well known and disclosed by Gao.

In accordance with Gao reference entirety, Gao discloses a widesense nonblocking switching networks (WNSN) comprising, among other things, the limitation of "*wherein each of the plurality of physical center stage switch circuits is comprised of a second three-stage switch*" (see Fig. 2; element 220) to provide multirate widesense nonblocking switching networks.

It would have been obvious to those skilled in the art at the time of the invention was made having the references readily available to incorporate Gao's WNSN into Zola's network to arrive the claimed invention with a motivation to provide multirate widesense nonblocking switching networks ('922, col. 2, lines 54-60).

Allowable Subject Matter

7. Claims 21, 22 and 24 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, considered individually or in combination, fails to fairly show or suggest the claimed invention of base claim 16 and further limit with novel and unobvious limitations in a manner as recited in the dependent claims 21-22 and 24.

Response to Arguments

9. Applicant's arguments filed 06/16/05 have been fully considered but they are not persuasive.

In the Remarks, on page 8, first paragraph of the outstanding response pertaining the rejection of newly amended claim 16 to include limitation of "*a Looping Algorithm is used as a control algorithm for the switch*", Applicants argue the prior art of Zola fails to teach such limitation.

In response Examiner respectfully disagrees and asserts the missing limitation from Zola reference is well known and taught by Andresen as clearly pointed out in the Office Action as discussed above.

On page 8, second paragraph continues to page 9, third paragraph, Applicants argue the Zola reference fails to teach "*the physical center stage switch circuits may be configured, represented, or otherwise controlled as a plurality of logical center stage switch circuits. Instead, Zola only shows the physical arrangement of the center stage switches 201, 202, etc.*"

In response Examiner respectfully disagrees and asserts the Zola reference, as clearly pointed out in the Office Action, does indeed teach the claimed limitation in a manner as recited in the claim. There is no doubt that Zola teaches Clos-type network

switch (*col. 1, lines 64-65*) having 2N-1 center stage switches, input stage and output stage (Fig. 2, col. 3, line 38 and col. 4, line 4). Clos-type network belongs to a class of networks called permute or permutation networks because they are adapted or capable of connecting plural inputs to plural outputs in an arbitrary manner. Moreover, the Clos-type network switch can be generated in a recursive way. In other words, by its nature, the center stage of the Zola's switch does implicitly and inherently anticipate the claimed limitation in a manner as recited in the claim, contradistinction to the Applicants' argument.

Examiner believes an earnest attempt has been made in addressing all of the Applicants' arguments. Due to the amendment fails to place the application in a favorable condition for allowance and the arguments are not persuasive, the rejection is maintained.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is 571-272-3164. The examiner can normally be reached on 7:00AM-3:30PM, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FRANK DUONG
PRIMARY EXAMINER

August 22, 2005